Attorney Docket No. NL 030715 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant(s): Roger Cuppens
Group Art Unit: 2824
Serial No. 10/560,677
Confirmation No. 8560
Filed: December 14, 2005
Examiner: Yang, Han
For: NON-VOLATILE STATIC MEMORY CELL

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Sir/Madam:

This brief is in furtherance of Applicant's Notice of Appeal filed on November 5, 2008, appealing the decision of the Examiner dated August 4, 2008 finally rejecting claims 1-5 and 7-12.

I. Real Party in Interest

The real party in interest in this appeal is NXP B.V., High Tech Campus 60, 5656 AG Eindhoven, The Netherlands.

II. Related Appeals and Interferences

There are currently no related appeals or interference proceedings in progress that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the present Appeal.

III. Status of Claims

Claims 1-10 were originally filed on December 14, 2005. In an Office Action response filed on February 4, 2008, claim 6 was canceled, claims 1-5, 7 and 8 were amended, and claims 11 and 12 were added. Claims 1-5 and 7-12 stand finally rejected and form the subject matter of the present appeal.

Claims 1-5 and 7-12 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 4,527,255 ("Keshtbod") in view of U.S. Patent No. 6,363,011 ("Hirose et al.")

This Appeal is made with regard to pending claims 1-5 and 7-12.

IV. Status of Amendments

No amendments were filed subsequent to final rejection.

V. Summary of Claimed Subject Matter

The claimed invention is a memory device, which can be used in a reconfigurable programmable logic device such as a field programmable gate array (See lines 4-5 on page 4 of specification).

According to an embodiment, as recited in the independent claim 1, a memory device comprises, in a single integrated circuit package, a static memory means (10, 12) defining at least first and second nodes communicatively connected with read and/or write data lines (See Fig. 3 and lines 8-10 on page 6 of the specification), and at least one non-volatile memory means (14, 16) associated with the static memory means, and writing data stored therein to the static memory means (See Fig. 3 and lines 16-19 on page 6 of the specification). The non-volatile memory means (14, 16) comprises a first non-volatile element (14) having a control gate connected to a first node and a source connected to a second node, and a second non-volatile element (16) having a control gate connected to the second node and a source connected to the first node, the drain of each non-volatile element being connected by means of a respective transistor (18, 20) to a supply means (See Fig. 3 and lines 10-13 on page 6 of the specification). The respective transistors (18, 20) are arranged to isolate the drains of the first and second non-volatile elements (14, 16) from the supply means during a program cycle of the memory device (See Fig. 3 and lines 14-15 on page 6 of the specification). The static memory means (10, 12) comprises a pair of cross-coupled inverters (See Fig. 3 and lines 8-9 on page 6 of the specification).

VI. Grounds of Rejection to be Reviewed on Appeal

Whether claims 1-5 and 7-12 are unpatentable under 35 U.S.C. §103(a) over Keshtbod in view of Hirose et al.

VII. Argument

In the Final Office Action of August 4, 2008, the Examiner rejected claims 1-5 and 7-12 under 35 U.S.C. §103(a) as allegedly being unpatentable over Keshtbod in view of Hirose et al. However, the Examiner has failed to establish a *prima facie* case of obviousness for claims 1-5 and 7-12, as explained below. Thus, the pending claims 1-5 and 7-12 are not obvious in view of the cited references of Keshtbod and Hirose et al.

A. Rejection of Independent Claim 1 Under 35 U.S.C. §103(a)

The Examiner has rejected the independent claim 1 under 35 U.S.C. 103(a) as allegedly being unpatentable over Keshtbod in view of Hirose et al. However, the Examiner has failed to establish a *prima facie* case of obviousness for the independent claim 1. Thus, the independent claim 1 cannot be rendered obvious in view of the cited references of Keshtbod and Hirose et al.

The Examiner admits on page 4 of the Final Office Action that the cited reference of Keshtbod does not disclose that "the static memory means comprises a pair of cross-coupled inverters." The Examiner then states that "Hirose et al. teaches the static memory (**Fig. 4, #4**) means comprises a pair of cross-coupled inverters (**Fig. 1, #45, #45'**)." The Examiner then alleges that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hirose et al. to the teaching of Keshtbod such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells."

First, Applicant does not fully understand the statement "such that the reading process of six transistors SRAM cells is easier than four transistor SRAM cells," which appears to be the alleged motivation to apply the inverters 45 and 45' of Hirose et al. to the bi-stable memory cell 30 of Keshtbod. This statement seems to suggest that the reading process of six transistors SRAM cells (presumably, the resulting memory cell) is somehow easier than the reading process of four transistors SRAM cells. Applicant fails to see how the reading process involving more transistors can be easier than the reading process involving fewer transistors. "The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." MPEP §2142. In the case at hand, the Examiner has not provided a clear articulation of the reason(s) why it is obvious to apply the teachings of Hirose et al. to the teachings of Keshtbod. Thus, the Examiner has not provided sufficient support to render the independent claim 1 obvious.

Second, there is no reasonable expectation of success in applying the teachings of Hirose et al. to the teachings of Keshtbod by presumably modifying the bi-stable memory cell 30 of Keshtbod using the inverters 45 and 45' of Hirose et al. The prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant notes herein that parts of one circuit cannot just be added to another circuit without knowing how those parts will function in the latter circuit. In certain situations, it cannot be known unless simulations are performed. In the case at hand, there is no reasonable expectation that adding the inverters 45 and 45' of Hirose et al. into the bi-stable memory cell 30 of Keshtbod would be successful since the inverters 45 and 45' of Hirose et al. are used with transistors 43 and 43', which are configured differently than transistors Q3 and Q4 of the bi-stable memory cell 30 of Keshtbod. Furthermore, the inverters 45 and 45' and the transistors 43 and 43' of Hirose et al. require various signals, which not used in the bi-stable memory cell 30 of Keshtbod. Thus, there is no reasonable expectation that the inverters 45 and 45' of Hirose et al. will function properly with the transistors Q3 and Q4 of the bi-stable memory cell 30 of Keshtbod.

Applicant also notes herein that the Examiner has not provided any details as to how to apply the teachings of Hirose et al. to the bi-stable memory cell 30 of Keshtbod. That is, the Examiner has not provided any details regarding how the bi-stable memory cell 30 of Keshtbod should be modified in view of the teachings of Hirose et al., i.e., the various electrical connections between the electrical components of the proposed memory cell. Thus, Applicant cannot fully address the issue of whether there is or is not reasonable expectation to make the proposed modifications.

Third, even assuming that there is reasonable expectation of success, the principle of operation of the memory cell of Keshtbod will be changed with the proposed modification. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being

modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The inclusion of the inverters 45 and 45' of Hirose et al. to the bi-stable memory cell 30 of Keshtbod would presumably require a Src signal, which is applied to the inverters 45 and 45', as illustrated in Fig. 5 of Hirose et al. In addition, as shown in Fig. 5, the inverters 45 and 45' also require Sel and In/ signals, which are not provided in the bi-stable memory cell 30 of Keshtbod. Since the bi-stable memory cell 30 of Keshtbod does not uses such signals for operation, the principle of operation of the memory cell of Keshtbod would need to be changed if the inverters 45 and 45' of Hirose et al. are included in the bi-stable memory cell 30 of Keshtbod. Thus, since the proposed modification of the bi-stable memory cell 30 of Keshtbod would change the principle of operation of the bi-stable memory cell, the teachings of Keshtbod and Hirose et al. are not sufficient to render the independent claim 1 *prima facie* obvious.

For all the above reasons, the Examiner has failed to establish a *prima facie* case of obviousness for the independent claim 1. Thus, the independent claim 1 cannot be rendered obvious in view of the cited references of Keshtbod and Hirose et al.

B. Rejection of Dependent Claims 2-5 and 7-12 Under 35 U.S.C. §103(a)

Each of the dependent claims 2-5 and 7-12 depends on the independent claim 1. As such, these dependent claims include all the limitations of the independent claim 1. Therefore, these dependent claims are allowable for the same reasons as the independent claim 1. Furthermore, each of these dependent claims may be allowable for additional reasons.

With respect to the dependent claim 11, the Examiner admits on page 7 of the Final Office Action that "Keshtob is silent with respect to gates of the respective transistors are connected together to receive a common signal." However, the Examiner then asserts that "Hirose et al. teaches gates of the

respective transistors are connected together to receive a common signal **(Fig. 5, #404)**" and that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hirose et al. to the teaching of Keshtob such that it's easy to control nonvolatile memory cells with common wordline." As shown in Fig. 5 of Hirose et al., the transistors 43 and 43' requires a Cg signal, which is not provided in Keshtbod. The Cg signal is presumably used to control both the transistors 43 and 43'. Thus, if the gates of the transistors Q5 and Q6 of Keshtbod are connected together, as taught in Hirose et al., the principle of operation of the bi-stable memory cell of Keshtbod would change since the resulting memory cell would need an extra signal and the transistors Q5 and Q6 may not independently turn on and off as needed in the original bi-stable memory cell 30 of Keshtbod. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for the dependent claim 11.

SUMMARY

With respect to the independent claim 1, the Examiner has failed to establish a *prima facie* case of obviousness because (1) the Examiner has not provided a valid rationale for combining the teachings of Keshtbod and Hirose et al., (2) there is no reasonable expectation of success to modify the bi-stable memory cell 30 of Keshtbod in the manner suggested by the Examiner, and (3) the principle of operation of the memory cell of Keshtbod will be changed with the proposed modification. The dependent claims 2-5 and 7-12 are also not obvious over the cited references of Keshtbod and Hirose et. for at least the same reasons as the independent claim 1.

For all the foregoing reasons, it is earnestly and respectfully requested that the Board of Patent Appeals and Interferences reverse the rejections of the Examiner regarding claims 1-5 and 7-12, so that this case may be allowed and pass to issue in a timely manner.

Respectfully submitted,
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VIII. Claims Appendix

1. A memory device comprising, in a single integrated circuit package:

a static memory means defining at least first and second nodes communicatively connected with read and/or write data lines; and

at least one non-volatile memory means associated with said static memory means, and writing data stored therein to said static memory means; said non-volatile memory means comprising a first non-volatile element having a control gate connected to a first node and a source connected to a second node, and a second non-volatile element having a control gate connected to the second node and a source connected to the first node, the drain of each non-volatile element being connected by means of a respective transistor to a supply means; characterized in that said respective transistors are arranged to isolate the drains of the first and second non-volatile elements from the supply means during a program cycle of the memory device,

wherein the static memory means comprises a pair of cross-coupled inverters.

2. A memory device according to claim 1, wherein said non-volatile memory elements comprise embedded flash or EEPROM elements.

3. A memory device according to claim 1, wherein said non-volatile memory elements comprise double or single poly floating gate type memory cells.

4. A memory device according to claim 1, wherein said non-volatile memory elements comprise devices which can be programmed and erased by means of tunneling of charges.

5. A memory device according to claim 1, wherein the non-volatile memory elements are programmed with opposite data.

6. (canceled).

7. A memory device according to claim 1, wherein one or more respective selection transistors are provided, by means of which the nodes are communicatively coupled to the read and/or write lines.

8. A memory device according to claim 1, including one or more isolation transistors.

9. A reconfigurable programmable logic device including a memory device according to claim 1.

10. A field programmable gate array including a memory device according to claim 1.

11. A memory device according to claim 1, wherein gates of the respective transistors are connected together to receive a common signal.

12. A memory device according to claim 1, wherein each of the cross-coupled inverters includes a pair of transistors, gates of the transistors of a first inverter of the cross-coupled inverters being connected to the second non-volatile element, gates of the transistors of a second inverter of the cross-coupled inverters being connected to the first non-volatile element.

IX. Evidence Appendix

NONE

X. Related Proceedings Appendix

NONE